TEMIC

Siliconix

SMD/SMU15N05

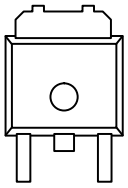
N-Channel Enhancement-Mode Transistors

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
50	0.10	15

TO-252



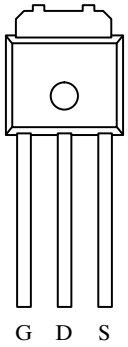
Drain connected to Tab

G D S

Top View

Order Number: SMD15N05

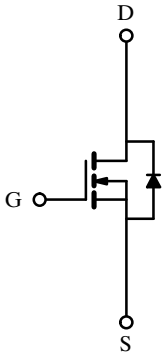
TO-251



G D S

Top View

Order Number: SMU15N05



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	SMD15N05	SMU15N05	Unit
Drain-Source Voltage		V_{DS}	50	50	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current[b]	T_A = 25°C	I_D	3.3[b]	2.3[c]	A
	T_A = 100°C		1.9[b]	1.3[c]	
Pulsed Drain Current (maximum current limited by package)		I_{DM}	24	24	
Power Dissipation	T_C = 25°C	P_D	40	40	W
	T_A = 25°C		2.0[b]	1.0[c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Free Air, PC Board Mount	R_{thJA}	50	60	°C/W
Junction-to-Ambient Free Air, Vertical Mount			125	
Junction-to-Case	R_{thJC}		3.0	

Notes:
a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
b. Surface mounted on PC board.
c. Free air, vertical mount.

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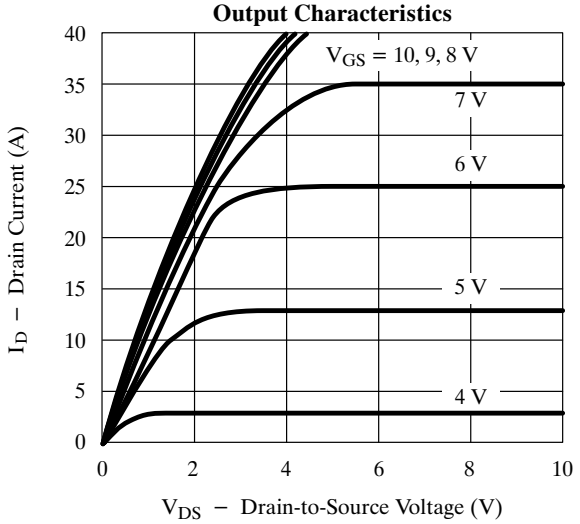
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V				25	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C				250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V		15			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 7.5 A			0.07	0.10	Ω
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C			0.13	0.18	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 7.5 A		3.0	4.8		S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz			550		pF
Output Capacitance	C_{oss}				320		
Reverse Transfer Capacitance	C_{rss}				100		
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 15 A			15	30	nC
Gate-Source Charge[c]	Q_{gs}				3.5		
Gate-Drain Charge[c]	Q_{gd}				5		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1.67 Ω I_D ≃ 15 A, V_{GEN} = 10 V, R_G = 25 Ω			15	30	ns
Rise Time[c]	t_r				50	85	
Turn-Off Delay Time[c]	$t_{d(off)}$				80	90	
Fall Time[c]	t_f				80	110	
Source-Drain Diode Ratings and Characteristics							
Continuous Current	I_S		SMD15N05			3.3	A
			SMU15N05			1.0	
Pulsed Current	I_{SM}					24	
Forward Voltage[b]	V_{SD}	I_F = 3.3 A, V_{GS} = 0 V			1.8	2.3	V
Reverse Recovery Time	t_{rr}	I_F = 3.3 A, dI_F/dt = 100 A/µs			65		ns
Reverse Recovery Charge	Q_{rr}				0.16		µC

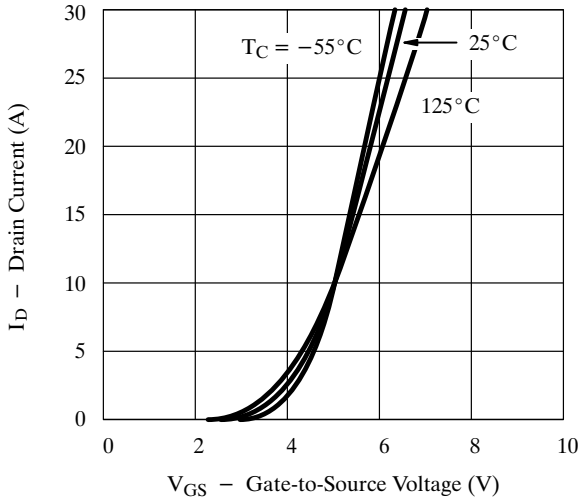
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

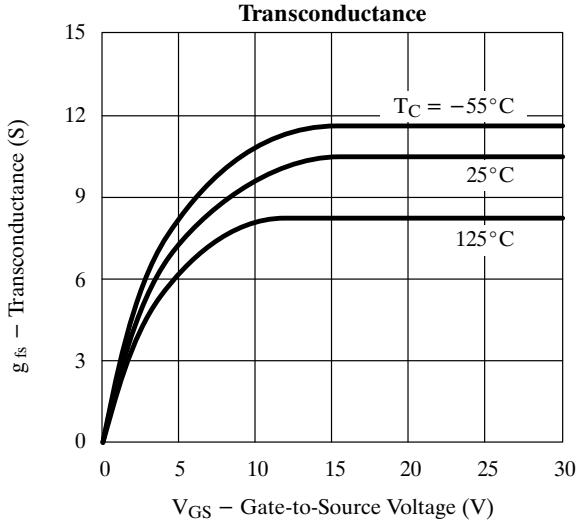
Output Characteristics



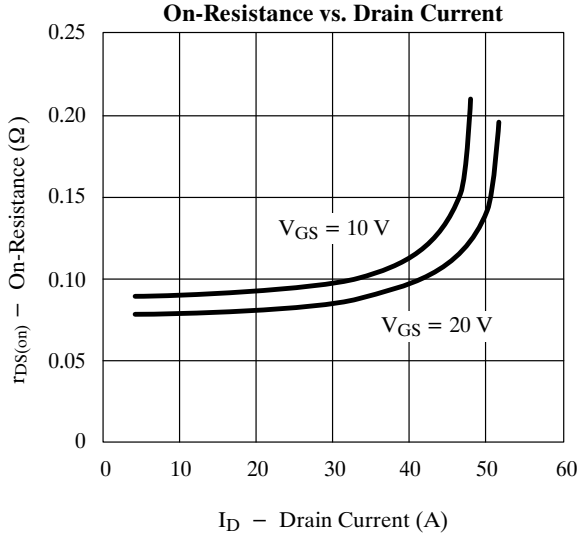
Transfer Characteristics



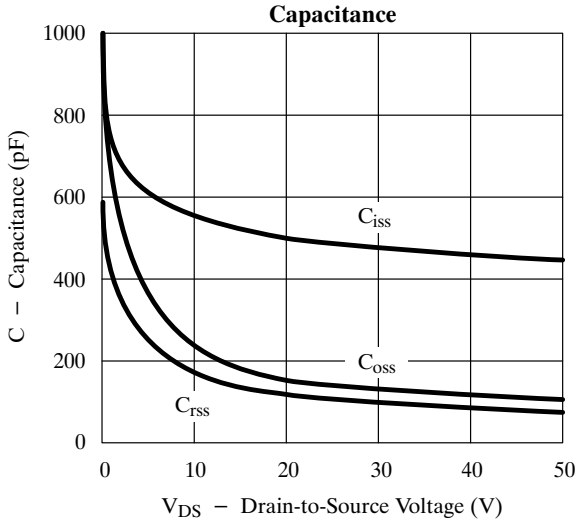
Transconductance



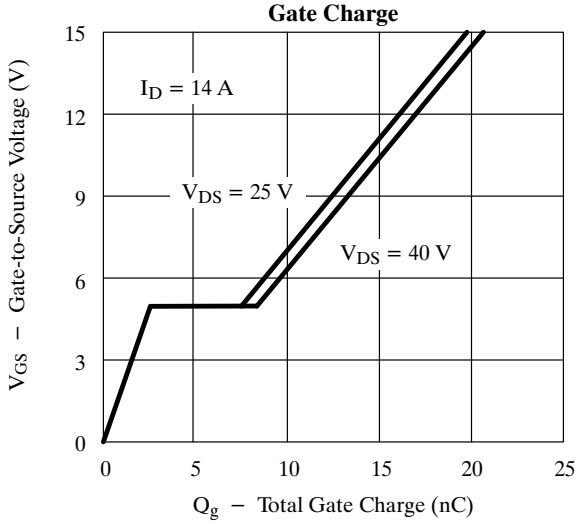
On-Resistance vs. Drain Current



Capacitance



Gate Charge



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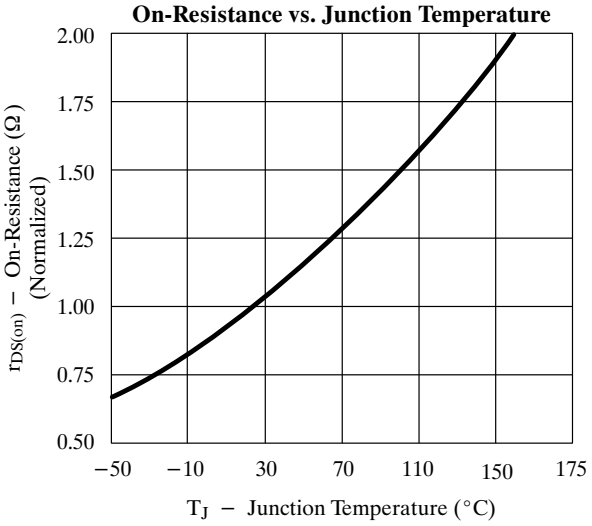
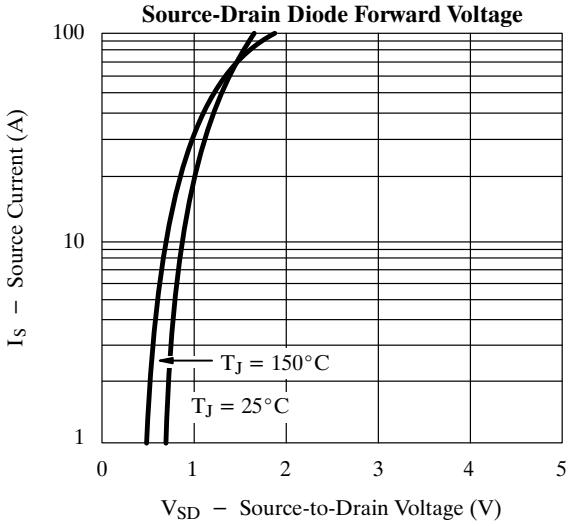
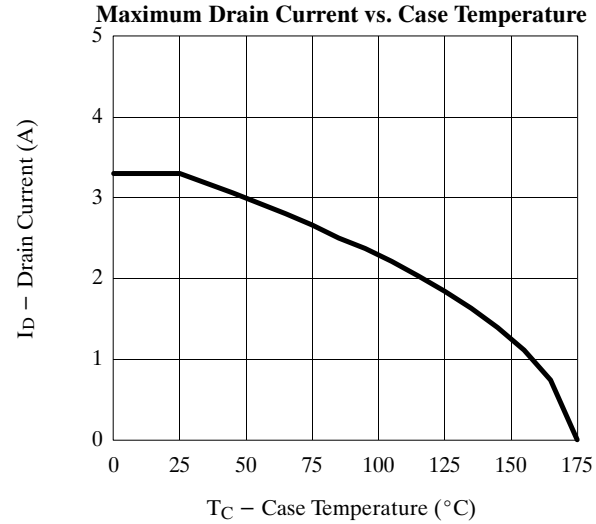
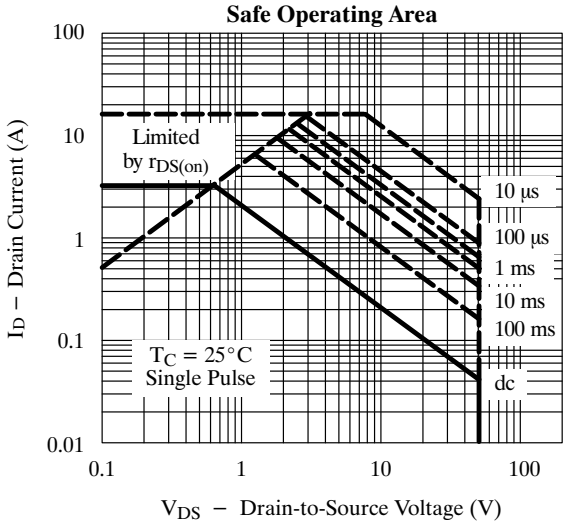
Typical Characteristics (25°C Unless Otherwise Noted)

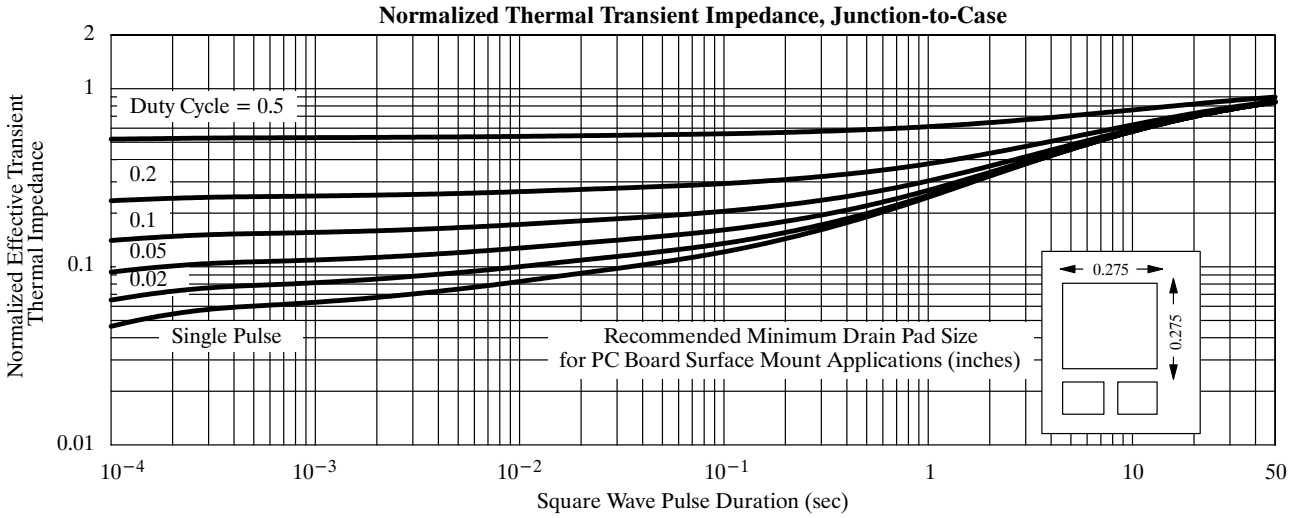




Thermal Ratings[a]







a. Surface Mounted on PC Board.